1117.40737X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: SCHETELIG, et al

Serial No.: Not yet assigned

Filed: October 19, 2001

For: METHOD AND DEVICE FOR IDENTIFYING A DATA PACKET IN A DATA STREAM

Group: Not yet assigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

October 19, 2001

Sir:

Prior to examination, please amend the above-identified application as follows.

IN THE SPECIFICATION

Please amend the specification as follows:

Please insert the following title on the page 1 of the specification: -- METHOD AND DEVICE FOR IDENTIFYING A DATA PACKET IN A DATA STREAM --.

Please insert before the first line of the specification the following:

-- CROSS REFERENCE TO RELATED APPLICATION

The present application is related to application Serial No. ________________, filed October 19, 2001, entitled ''METHOD

AND DEVICE FOR CONTROLLING DATA EXTRACTION FROM A DATA STREAM CONTAINING AT LEAST ONE DATA PACKET'', by M. Schetelig et al. --

Page 1, line 1, delete ''Description'' insert --Background of the Invention--.

IN THE CLAIMS

Page 21, line 1, delete ''Patent claims'' insert --What is claimed is:--

Please amend the claims as follows:

4. (Amended) Method according to Claim 2, wherein after a packet identification signal (P_d) has been generated the corresponding correlation value (c_v) is stored and scanning of the input signal (S_{in}), calculation of the d.c. voltage quota (dc) and comparison of the k-bit word corresponding to the input signal (S_{in}) with an expected k-bit synchronisation word to determine the correlation value (c_v) is still continued for a predeterminable period of time and a new packet identification signal (P_d) is generated if a newly determined correlation value (c_v) is greater than the correlation threshold value (C_{th}) and greater than the previously determined stored correlation value (c_v).

5. (Amended) Method according to claim 4, characterized to determine the k-bit word corresponding to the input signal (S_{in}) the input signal (S_{in}) is scanned in order to generate a sequence of scanned values (h_i) corresponding to the input signal (S_{in}) and a bit value (1 or 0) is allocated to each scanned value (h_i) of a selected multiplicity (k) of scanned values (h_i) as a function of the d.c. voltage quota (dc) of the input signal (S_{in}).

6. (Amended) Method according to claim 5, wherein the input signal (Sin) is scanned at a frequency (f_{sample}) which is chosen in such a way that the over-scanning rate (s_r) is at least equal to two ($S_r \geq 2$), that therefore at least two scanned values (h_i) are determined for each symbol and to form the k-bit word corresponding to the input signal (S_{in}) in each case only one scanned value (h_i) per symbol is selected.

7. (Amended) Method according to Claim 6, wherein the multiplicity (k) of scanned values (h_i) for forming the kbit word corresponding to the input signal (S_n) is selected from the sequence of scanned values (h_i) in such a way that the selected scanned values (h_i) within the sequence in each case are substantially the same distance apart.

8. (Amended) Method according to claim 7, wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) of the input signal (S_{in}) is chosen in such a way that the scanned values (h_i) correspond to areas in the expected k bit synchronisation word which substantially have the same number of bits with the value "0" and bits with the value "1" and the d.c. voltage quota (dc) is calculated as an average value of the scanned values (h_i)

9. (Amended) Method according to Claim 8, wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of at least one group of scanned values (h_i) in direct succession to one another, which correspond to several successive symbols.

10. (Amended) Method according to Claim 8, wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of two groups of scanned values (h_i), which are separated from one another by a multiplicity of scanned values (h_i).

11. (Amended) A device for identifying data packets in a data receiving stream with a delay line which has a number

(n) of storage places (), in which scanned values (h_i) of a demodulated digital input signal (S_{in}) are stored in series, a d.c. voltage quota determining circuit , which is connected to the delay line in order to calculate a d.c. voltage quota (dc) of the input signal (S_{in}) as an average value of a selected number of scanned values (h_i),

a decoding circuit connected to the delay line and the d.c. voltage quota determining circuit which compares a multiplicity (k) of scanned values (h_i) with the d.c. voltage quota (dc) in order to allocate a bit value (0 or 1) to each scanned value (h_i) and in this way to form a k-bit word corresponding to the input signal (S_{in})

a comparison and correlation calculating circuit which compares the k-bit word corresponding to the input signal with an expected k-bit synchronisation word and calculates a correlation value (c_v) for the k-bit word corresponding to the input signal (S_{in}) and

a correlation value comparison circuit which compares the correlation value (c_v) supplied by the comparison and correlation calculating circuit with a correlation threshold value (C_{th}) in order to supply a packet identification signal (P_d) if the correlation value (c_v) is greater than or equal to the correlation threshold value (C_{th}).

12. (Amended) A device according to Claim 11, wherein the number (n) of storage places (22.i) of the delay line corresponds to the number (k) of bits in the k-bit synchronisation word multiplied by the over-scanning rate (s_r), in other words with the number of scanned values (hi) per symbol.

13. (Amended) A device according to Claim 11, wherein the decoding circuit comprises a multiplicity (k) of comparison circuits, to which in each case is applied the d.c. voltage quota (dc) and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned value (h_i) with the d.c. voltage quota (dc) and to determine a bit value (1 or 0), so the k-bit word corresponding to the input signal (S_{in}) is applied to outputs (out(i)) of the decoding circuit.

14. (Amended) A device according to Claim 11, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element , wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line (, which is separated from the first storage place by a

multiplicity of storage places ,

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element , so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit is divided in the division circuit by a value (m_1 - m_2; m_3 - m_4) corresponding to the distance between the storage places in order to calculate the d.c. voltage quota (dc).

15. (Amended) Device according to Claim 14, wherein two addition circuits connected to storage places of the delay line are provided, the output signals of which are supplied to the division circuit via a further addition circuit .

16. (Amended) A device according to Claim 15, wherein the comparison and correlation calculating circuit connected to the decoding circuit and a register storing the expected k-bit synchronisation word, besides a multiplicity (k) of comparison circuits for comparing the k-bit word supplied by the decoding circuit and corresponding to the input signal with the k-bit synchronisation word, has a correlation element which adds a one for each coinciding bit pair in order to calculate the correlation value (c_v).

Please add new claims 17-21 as follows:

-- 17. Method according to Claim 3, wherein after a packet identification signal (P_d) has been generated the corresponding correlation value (c_v) is stored and scanning of the input signal (S_{in}), calculation of the d.c. voltage quota (dc) and comparison of the k-bit word corresponding to the input signal (S_{in}) with an expected k-bit synchronisation word to determine the correlation value (c_v) is still continued for a predeterminable period of time and a new packet identification signal (P_d) is generated if a newly determined correlation value (c_v) is greater than the correlation threshold value (C_{th}) and greater than the previously determined stored correlation value (c_v).

18. Method according to Claim 9, wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of two groups of scanned values (h_i), which are separated from one another by a multiplicity of scanned values (h_i).

19. A device according to Claim 12, wherein the decoding circuit comprises a multiplicity (k) of comparison circuits, to which in each case is applied the d.c. voltage quota

(dc) and each of which is connected to one of the storage places of the delay line in order to compare the respective scanned value (h_1) with the d.c. voltage quota (dc) and to determine a bit value (1 or 0), so the k-bit word corresponding to the input signal (S_{in}) is applied to outputs (out(i)) of the decoding circuit.

20. A device according to Claim 12, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element , wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places,

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element , so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit is divided in the division circuit by a value (m_1 - m_2; m_3 - m_4) corresponding to the distance between the storage places in order to calculate the d.c. voltage quota (dc).

21. A device according to Claim 13, wherein the d.c. voltage quota determining circuit has at least one addition circuit and one division circuit connected to the output of the addition circuit via a holding element, wherein one input of the addition circuit is connected to a first storage place of the delay line and another input is connected to a second storage place of the delay line which is separated from the first storage place by a multiplicity of storage places,

the input which is connected to the second storage place is negated and the output of the addition circuit is fed back to a third input via the holding element, so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit is divided in the division circuit by a value (m_1 - m_2; m_3 - m_4) corresponding to the distance between the storage places in order to calculate the d.c. voltage quota (dc). --

IN THE ABSTRACT

Please replace the Abstract with the attached new Abstract.

REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned ''**Version with markings to show changes made**''.

Entry of the above amendments prior to examination is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (1117.40737X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Carl I. Brundidge
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ABSTRACT

The invention relates to a method and a device for identifying a data packet in a data stream, in which by means of a d.c. voltage quota determining circuit the d.c. voltage quota (dc) for a demodulated digital input signal (S_{in}) is calculated, in which a k-bit word is allocated to the input signal (S_{in}), in that for each symbol of the input signal (S_{in}) corresponding to a bit a bit value (1 or 0) is determined by a decoding circuit as a function of the d.c. voltage quota (dc), in which the k-bit word corresponding to the input signal (S_{in}) is compared by a comparison and correlation calculating circuit with an expected k-bit synchronisation word in order to determine a correlation value (c_v) and in which a packet identification signal (P_d) is generated by a correlation value comparison circuit if the correlation value (c_v) is greater than a correlation threshold value (C_{th}) Calculation of the d.c. voltage quota (dc) is therein repeated continually at least until a packet identification signal (P_d) indicates that a data packet is being received.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please amend the specification as follows:

Please insert the following title on the page 1 of the specification: -- METHOD AND DEVICE FOR IDENTIFYING A DATA PACKET IN A DATA STREAM --.

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Page 1, line 1, delete ''Description'' insert --Background of the Invention--.

IN THE CLAIMS

Page 21, line 1, delete ''Patent claims'' insert --What is claimed is:--

Please amend the claims as follows:

4. (Amended) Method according to Claim 2 ~~or 3~~, ~~characterised in that~~ wherein after a packet identification

signal (P_d) has been generated the corresponding correlation value (c_v) is stored and scanning of the input signal (S_{in}), calculation of the d.c. voltage quota (dc) and comparison of the k-bit word corresponding to the input signal (S_{in}) with an expected k-bit synchronisation word to determine the correlation value (c_v) is still continued for a predeterminable period of time and a new packet identification signal (P_d) is generated if a newly determined correlation value (c_v) is greater than the correlation threshold value (C_{th}) and greater than the previously determined stored correlation value (c_v).

5. (Amended) Method according to ~~one of the preceding claims~~ claim 4, ~~characterised~~characterized ~~in that~~ to determine the k-bit word corresponding to the input signal (S_{in}) the input signal (S_{in}) is scanned in order to generate a sequence of scanned values (h_i) corresponding to the input signal (S_{in}) and a bit value (1 or 0) is allocated to each scanned value (h_i) of a selected multiplicity (k) of scanned values (h_i) as a function of the d.c. voltage quota (dc) of the input signal (S_{in}).

6. (Amended) Method according to ~~one of claims 1 to~~ claim 5, ~~characterised in that~~ wherein the input signal (Sin) is scanned at a frequency (f_{sample}) which is chosen in such a way

that the over-scanning rate (s_r) is at least equal to two ($S_r \geq 2$), that therefore at least two scanned values (h_i) are determined for each symbol and to form the k-bit word corresponding to the input signal (S_{in}) in each case only one scanned value (h_i) per symbol is selected.

7. (Amended) Method according to Claim 6, ~~characterised in that~~ wherein the multiplicity (k) of scanned values (h_i) for forming the kbit word corresponding to the input signal (S_n) is selected from the sequence of scanned values (h_i) in such a way that the selected scanned values (h_i) within the sequence in each case are substantially the same distance apart.

8. (Amended) Method according to ~~one of the preceding claims~~ claim 7, ~~characterised in that~~ wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) of the input signal (S_{in}) is chosen in such a way that the scanned values (h_i) correspond to areas in the expected k bit synchronisation word which substantially have the same number of bits with the value "0" and bits with the value "1" and the d.c. voltage quota (dc) is calculated as an average value of the scanned values (h_i)

9. (Amended) Method according to Claim 8, ~~characterised in~~

~~that~~ wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of at least one group of scanned values (h_i) in direct succession to one another, which correspond to several successive symbols.

10. (Amended) Method according to Claim 8 ~~or 9~~, ~~characterised in that~~ wherein the number (1) of scanned values (h_i) for calculating the d.c. voltage quota (dc) consists of two groups of scanned values (h_i), which are separated from one another by a multiplicity of scanned values (h_i).

11. (Amended) A ~~Device~~ device for identifying data packets in a data receiving stream with a delay line ~~(22)~~ which has a number (n) of storage places (~~22.i~~), in which scanned values (h_i) of a demodulated digital input signal (S_{in}) are stored in series, a d.c. voltage quota determining circuit ~~(30)~~, which is connected to the delay line ~~(22)~~ in order to calculate a d.c. voltage quota (dc) of the input signal (S_{in}) as an average value of a selected number ~~(1)~~ of scanned values (h_i),

a decoding circuit ~~(37)~~ connected to the delay line ~~(22)~~ and the d.c. voltage quota determining circuit ~~(30)~~ which compares a multiplicity (k) of scanned values (h_i) with the d.c. voltage quota (dc) in order to allocate a bit value (0 or 1) to

each scanned value (h_i) and in this way to form a k-bit word corresponding to the input signal (S_{in})

a comparison and correlation calculating circuit ~~(41)~~ which compares the k-bit word corresponding to the input signal with an expected k-bit synchronisation word and calculates a correlation value (c_v) for the k-bit word corresponding to the input signal (S_{in}) and

a correlation value comparison circuit ~~(43)~~ which compares the correlation value (c_v) supplied by the comparison and correlation calculating circuit ~~(41)~~ with a correlation threshold value (C_{th}) in order to supply a packet identification signal (P_d) if the correlation value (c_v) is greater than or equal to the correlation threshold value (C_{th}).

12. (Amended) A ~~Device~~ device according to Claim 11, ~~characterised in that~~ wherein the number (n) of storage places (22.i) of the delay line ~~(22)~~ corresponds to the number (k) of bits in the k-bit synchronisation word multiplied by the over-scanning rate (s_r), in other words with the number of scanned values (hi) per symbol.

13. (Amended) A ~~Device~~ device according to Claim 11 ~~or 12~~, ~~characterised in that~~ wherein the decoding circuit ~~(37)~~ comprises a multiplicity (k) of comparison circuits, to which in each case

is applied the d.c. voltage quota (dc) and each of which is connected to one of the storage places ~~(22.i)~~ of the delay line ~~(22)~~ in order to compare the respective scanned value (h_i) with the d.c. voltage quota (dc) and to determine a bit value (1 or 0), so the k-bit word corresponding to the input signal (S_{in}) is applied to outputs (out(i)) of the decoding circuit.

14. (Amended) A ~~Device~~ device according to Claim 11, ~~12 or 13~~, ~~characterised in that~~ wherein the d.c. voltage quota determining circuit ~~(30)~~ has at least one addition circuit ~~(33)~~ and one division circuit ~~(36)~~ connected to the output of the addition circuit ~~(33)~~ via a holding element ~~(34)~~, wherein one input of the addition circuit ~~(33)~~ is connected to a first storage place ~~(22.m$_1$, 22.M$_3$)~~ of the delay line ~~(22)~~ and another input is connected to a second storage place ~~(22 M$_2$, 22 M$_4$)~~ of the delay line (~~22)~~, which is separated from the first storage place ~~(22.m$_1$, 22.M$_3$)~~ by a multiplicity of storage places ~~(22.i)~~,the input which is connected to the second storage place ~~(22.m$_2$, 22.m$_4$)~~ is negated and the output of the addition circuit ~~(33)~~ is fed back to a third input via the holding element ~~(34)~~, so that with each addition the result of the preceding addition is added on and wherein the sum supplied by the holding circuit ~~(34)~~ is divided in the division circuit by a value (m_1 - m_2; m_3 - m_4) corresponding to the distance between

the storage places ~~(22.m_1, 22.m_3; 22.m_2, 22.m_4)~~ in order to calculate the d.c. voltage quota (dc).

15. (Amended) Device according to Claim 14, ~~characterised in that~~ wherein two addition circuits ~~(33)~~ connected to storage places ~~(22.m_1, 22.m_3; 22.m_2, 22.m_4)~~ of the delay line ~~(22)~~ are provided, the output signals of which are supplied to the division circuit ~~(36)~~ via a further addition circuit ~~(35)~~.

16. (Amended) A ~~Device~~ device according to ~~one of the preceding claims~~, ~~characterised in that~~ wherein the comparison and correlation calculating circuit ~~(41)~~ connected to the decoding circuit ~~(37)~~ and a register ~~(42)~~ storing the expected k-bit synchronisation word, besides a multiplicity (k) of comparison circuits for comparing the k-bit word supplied by the decoding circuit ~~(37)~~ and corresponding to the input signal with the k-bit synchronisation word, has a correlation element which adds a one for each coinciding bit pair in order to calculate the correlation value (c_v).